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09/963,894	09/25/2001	Akimitsu Shimamura	10873.785US01	9424

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,894	SHIMAMURA, AKIMITSU	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *22 January 2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 have been considered.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Figures 1, 2, and 6, elements 14, 15, 16, 17, 18, 19, 29, 35, 36, and 37; Figure 7, elements 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, and 119. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. Specification contains numerous grammatical errors, please review and correct accordingly. Examples are:

a. Page 10, line 4 please correct "output of the ALU21 matches" to read --output of the ALU 21--

b. Page 10, line 7 please correct "output of the EXE7 of the pipeline execution stage" to read --output of the EXE 7 of the pipeline execution stage--

c. Page 10, line 23 please correct "from the ALU22" to read --from the ALU 22—

5. The claims are objected to because they contain numerous grammatical errors. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 11-16. and 24-26 are rejected under 35 U.S.C. 102(b) as being taught by Sager et al., U.S. Patent Number 5,828,868 (herein referred to as Sager).

8. Referring to claim 1, Sager has taught a computer system employing a pipeline operation wherein the pipeline is driven by a high clock frequency higher than a low clock frequency by which a critical path instruction in processing data can be executed correctly, comprising:

a. A high frequency ALU driven by a pipeline clock frequency, a low frequency ALU driven by a low clock frequency lower than the pipeline clock frequency, by which low clock frequency the critical path instruction can be executed correctly (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6), wherein

b. If the high frequency ALU can execute an instruction correctly, the execution result of the high frequency ALU is outputted as an execution result of a pipeline execution stage (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6),

c. If the high frequency ALU can not execute the instruction correctly, the execution result of the low frequency ALU is outputted as an execution result of the pipeline execution stage (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6).

9. Referring to claim 2, Sager has taught

a. Wherein the low frequency ALU is composed of plural low frequency ALUs (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6);

b. The low frequency ALU in charge of each execution stage is switched in turn, and each low frequency ALU in charge executes an execution stage instruction in charge correctly by the low clock frequency which is equal to or lower than the clock frequency for operating a critical path instruction correctly (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6).

10. Referring to claim 14, Sager has taught a method for controlling a pipeline operation in a computer system wherein the pipeline is driven by a high clock frequency higher than a low

clock frequency by which a critical path instruction in processing data can be executed correctly, comprising:

a. Using a high frequency ALU driven by a pipeline clock frequency, a low frequency ALU driven by a low clock frequency lower than the pipeline clock frequency, by which low clock frequency the critical path instruction can be executed correctly (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6), wherein

b. If the high frequency ALU can execute an instruction correctly, the execution result of the high frequency ALU is outputted as an execution result of a pipeline execution stage (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6),

c. If the high frequency ALU can not execute the instruction correctly, the execution result of the low frequency ALU is outputted as an execution result of the pipeline execution stage (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6).

11. Referring to claim 15, Sager has taught

a. Wherein the low frequency ALU is composed of plural low frequency ALUs (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6);

b. Switching the low frequency ALU in charge of each execution stage in turn, and assigning each low frequency ALU in charge for an execution stage instruction in charge to execute it correctly by the low clock frequency which is equal to or lower than the clock frequency for operating a critical path instruction correctly (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6).

12. Referring to claims 3 and 16, Sager has taught

a. Wherein the number of the plural low frequency ALUs is "n" when the pipeline clock frequency is "n" times of the clock frequency by which the critical path instruction can be executed correctly (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6),

b. Each of the "n" pieces of the low frequency ALUs is in charge of "n" pieces of execution stages of pipeline in order respectively (Sager Abstract; column 1, lines

26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6).

13. Referring to claims 11 and 24, Sager has taught

a. Wherein the following amounts of two processes are compared when the pipeline clock frequency is increased and the number of the critical path instructions is increased, the one being an improved processor amount of the high frequency ALU and the other being a deteriorated process amount by increasing of the replacement process of the output of the low frequency ALU as the execution result of the pipeline execution stage when the high frequency ALU cannot execute the instruction correctly (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6),

b. Wherein, when the former is larger than the latter by the predetermined amount, the pipeline clock frequency is increased (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6).

14. Referring to claims 12 and 25, Sager has taught

a. Wherein the following amounts of two processes are compared when the pipeline clock frequency is decreased and the number of the critical path instructions is

decreased, the one being an deteriorated processor amount of the high frequency ALU if the pipeline clock frequency is lowers, and the other being an improved process amount by decreasing of the replacement process of the output of the low frequency ALU as the execution result of the pipeline execution stage when the high frequency ALU cannot execute the instruction correctly (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6),

b. Wherein, when the latter is larger than the former by the predetermined amount, the pipeline clock frequency is decreased (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6).

15. Referring to claim 13 and 26, Sager has taught

a. Plural ALUs, a data generation circuit generating test data as a critical path data, an execution time measurement circuit measuring critical path instruction in each ALU, and a detector detecting the fastest ALU that can execute the critical path instruction in a shortest time (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6),

b. Wherein, the ALU detected by the detector is selected as the high frequency ALU, and the other one ALU or plural ALUs is/are selected as the low frequency ALU/ALUs (Sager Abstract; column 1, lines 26-33; column 1, line 57 to column 2, line 39; column 3, line 32 to column 4, line 12; column 4, line 40 to column 5, line 7; column 5, lines 28-43 and 58-67; column 6, lines 19-50; Figure 3; Figure 4; Figure 5; and Figure 6).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 4-9 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sager et al., U.S. Patent Number 5,828,868 (herein referred to as Sager) in view of Kreitzer, U.S. Patent Number 5,253,349 (herein referred to as Kreitzer). Sager has not explicitly taught

a. Comparing the output of the high frequency ALU and the output of the low frequency ALU in charge of the same execution stage for the same instruction (Applicant's claims 4, 6, 8, 17, 19, and 21),

b. Wherein, the output of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when the compared result of the comparator indicates matching, the output of the high frequency ALU is determined as the execution result of the execution stage and the pipeline operation is continued, and when the compared result of the comparator indicates mismatching, the

output of the high frequency ALU is replaced with the output of the low frequency ALU as the execution result of the pipeline execution stage (Applicant's claims 4, 6, 8, 17, 19, and 21).

c. Wherein when the compared result of the comparator indicates mismatching, all stages of the pipeline are stopped until finished the replacement process in which the output of the low frequency ALU is selected as the execution result of the pipeline stage (Applicant's claims 5, 7, 9, 18, 20, and 22).

18. However, Sager has taught multiple ALUs with different clock frequencies and using the output of one of the ALUs (Sager Abstract; column 2, lines 1-50; column 4, lines 3-20; column 4, line 48 to column 5, line 15; column 5, lines 36-51; column 5, line 66 to column 6, line 8; column 6, lines 27-58; Figure 3; Figure 4; Figure 5; and Figure 6). Kreitzer has taught

a. Comparing the outputs of two devices (Kreitzer Abstract and column 1, lines 29-42 and 45-58);

b. Wherein, the output of one device is assumed as the result, and when the compared result of the comparator indicates matching, the output of one device is determined as the result and operation is continued, and when the compared result of the comparator indicates mismatching, the output of one device is replaced with the output of another device as the execution result of the pipeline execution stage (Kreitzer Abstract and column 1, lines 29-42 and 45-58); and

c. Wherein when the compared result of the comparator indicates mismatching, all stages of the pipeline are stopped until finished the replacement process in which

the output of another device is selected as the execution result of the pipeline stage (Kreitzer Abstract and column 1, lines 29-42 and 45-58).

19. A person of ordinary skill in the art at the time the invention was made, and as supported by Kreitzer, would have recognized that this type of comparison system shortens the execution times of certain instructions, thereby improving the processing efficiency (Kreitzer column 1, lines 40-42). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the comparison system of Kreitzer in the device of Sager to improve processor efficiency.

20. Claims 10 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sager et al., U.S. Patent Number 5,828,868 (herein referred to as Sager) in view of Kreitzer, U.S. Patent Number 5,253,349 (herein referred to as Kreitzer). Sager has taught a circuit varying the pipeline clock frequency (Sager Abstract; column 2, lines 1-50; column 4, lines 3-20; column 4, line 48 to column 5, line 15; column 5, lines 36-51; column 5, line 66 to column 6, line 8; column 6, lines 27-58; Figure 3; Figure 4; Figure 5; and Figure 6). Sager has not taught a counter counting the number of occurrences of the mismatching detection signal in a predetermined period. Ryan has taught a counter counting the number of occurrences of the mismatching detection signal in a predetermined period (Ryan column 1, lines 43-56). A person of ordinary skill in the art at the time the invention was made, and as supported by Ryan, would have recognized that counting the number of mismatches allows the determination of what type of error or fault has occurred (Ryan column 53-56) for correction, thereby ensuring the process has executed correctly. Therefore, it would have been obvious to a person of ordinary skill in the

art the time the invention was made to incorporate the counter of Ryan in the device of Sager to ensure correct processing of data.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Carnevale et al., U.S. Patent Number 3,656,123, has taught a system with an ALU with different clock frequencies.

b. Dockser, U.S. Patent Number 5,649,174, has taught a microprocessor which executes instructions of different cycle lengths.

c. Okamura, U.S. Patent Number 6,023,756, has taught multiple ALUs which execute at different clock cycle rates.

d. Sager et al., U.S. Patent Numbers 6,216,234 and 6,256,745, have taught multiple execution cores with separate clock frequencies.

e. Gorshtein et al., U.S. Patent Number 6,668,316, has taught multiple ALUs, which operate at different clock cycle rates, with selective output from the ALUs.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
September 20, 2004

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